



Attorney Docket: BHT/3230-63

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : TSUI  
Application No. : 10/625,516  
Filed : July 24, 2003  
Title : STRUCTURE OF METAL OXIDE SEMICONDUCTOR  
FIELD EFFECT TRANSISTOR  
Group Art Unit : 2813  
Examiner : C. Thompson  
Docket No. : BHT/3230-63

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT**

Sir:

In compliance with the duty of disclosure under 37 CFR 1.56, and 37 CFR 1.97-1.98, the documents listed on the attached form PTO-1449 are hereby made of record in this patent application. Copies of the listed documents are enclosed.

As this Information Disclosure Statement is being filed following the issuance of the first Official Action in this application, the appropriate fee is also enclosed, in order to have the enclosed references considered by the Examiner and made of record in the application.

08/03/2004 HLE333 00000065 10625516

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Respectfully submitted,

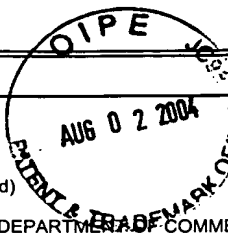
Date: August 2, 2004

By:

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FORM PTO 1449 (modified)

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICELIST OF REFERENCES CITED BY APPLICANT(S)  
(Use several sheets if necessary)ATTY DOCKET NO. **BHT/3230-63**APPLICATION NO. **10/625,516**APPLICANT **TSUI**FILING DATE **July 24, 2003**GROUP **2813**Date Submitted to PTO: **August 2, 2004**

## U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES/NO/ OR ABSTRACT

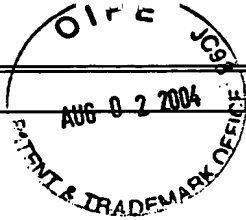
## OTHER DOCUMENT(S) (Including Author, Title, Date, Pertinent Pages, Etc.)

		<b>C.J. Koeneke, et al.; "Schottky MOSFET for VLSI"; in Dig. of IEDM, p. 367; 1981</b>
		<b>S.E. Swirhun et al.; "A VLSI Suitable Schottky Barrier CMOS Process"; IEEE, Trans. Electron Devices; Vol. ED-32, No. 2; p. 194; 1985</b>
		<b>B.Y. Tsui et al.; "A Novel Process For High-Performance Schottky Barrier PMOS"; J. Electrochem. Soc.; Vol. 136, No. 5; p. 1456; 1989</b>
		<b>C. Wang et al.; "Sub-50-nm PtSi Schottky Source/Drain p-MOSFETs"; in Proc. of Device Research Conf.; p/72; 1998</b>
		<b>C. Wang et al.; "Sub-50-nm PtSi Schottky Source/Drain Metal-Oxide-Semiconductor Field-Effect Transistors; Appl. Phys. Lett.; Vol. 74, No. 8; p. 1174; 1999</b>
		<b>W. Saitoh et al. ; "35 nm Metal Gate SOI-p-MOSFETs With PtSi Schottky Source/Drain"; in Proc. of Device Research Conf.; p. 30; 1999</b>
		<b>A. Itoh et al.; "Very Short Channel Metal-Gate Schottky Source/Drain SOI-PMOSFETs And Their Short Channel Effect"; in Proc. of Device Research Conf.; p. 77; 2000</b>
		<b>H.C. Lin et al.; "A Novel Implantless MOS Thin-Film Transistor With Simple Processing, Excellent Performance, and Ambipolar Operation Capability"; in Dig. of IEDM; p. 857; 2000</b>
		<b>K. Uchida et al.; "Enhancement Of Hot-Electron Generation Rate in Schottky Source Metal-Oxide-Semiconductor Field-Effect Transistors"; Appl. Phys. Lett.; Vol. 76, No. 26; p. 3992; 2000</b>

EXAMINER

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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



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